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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,566	10/31/2002	Yi-chen Chang	9747-US-PA	7637

31561 7590 04/18/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
FATAHI YAR, MAHMOUD	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/065,566	YI-CHEN CHANG	
	Examiner	Art Unit	
	Mike Fatahiyar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20, and 24-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1-5, 7, 8, 10, 12-16, 18-20 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiya et al(6,583,775) in view of Shigeta(6,091,385).

In regard to claim 1, Sekiya discloses a driving circuit, depicted in figure 1, for a display device having a plurality of pixels. See column 6, lines 30-32, disclosing, "there is provided an image display apparatus, comprising a plurality of pixels arranged in a matrix". Sekiya further discloses that driving circuit is used for driving the light-emitting device in each pixel. See column 10, lines 58-60, disclosing, "The light emitting element OLED emits light with a brightness value which varies depending upon the amount of current supplied thereto."

Sekiya further discloses that the driving circuit comprises a light-emitting device driving unit coupled to the light-emitting device for providing a driving current to the light-emitting device selectively. See column 10, lines 64-67, disclosing, "The second thin film transistor TFT2 controls the amount of current to be supplied to the light emitting element OLED in response to the brightness information written in the holding capacitor C".

Sekiya further discloses that the driving circuit comprises a discharging unit coupled to the light-emitting device driving unit for discharging light-emitting device according to the voltage level of a control signal. See column 11, lines 29-33, disclosing, "When a third thin film transistor TFT 3 is placed into an on state with the control signal, the corresponding holding capacitor Cs discharges and the gate-source voltage Vgs of the second thin film transistor TFT2 becomes 0 V. Consequently, the current to flow to the light emitting

element OLED is cut off." Sekiya, did not expressly detailed discharging the light emitting device.

Shigeta is cited to teach that it is well known to charge or discharge(64 and 66 respectively) a light emitting element(78) (see, co1.1, lines 65 -col.2, lines 4,46-57, co1.3, lines 30-50).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to have been motivated to incorporate the discharging method of Shigeta into the device of Sekiya, because this will allow to have uniform luminescence of individual pixels without requiring a back light and provide less weight.

In regard to claim 2, Sekiya discloses that the driving circuit may further include a light-emitting device selection unit coupled to the light-emitting device driving unit for receiving a scan signal and a data signal. See figure 1 and column 10, lines 60-63, disclosing, "The first active element TFT1 is controlled by the corresponding scanning line X and writes brightness information given thereto from the corresponding data line Y into the holding capacitor Cs included in the pixel PXL."

Sekiya further discloses that when the scan signal and the data signal are at logic level "1", the light-emitting device selection unit enables the light-emitting device driving unit to provide a driving current to the light-emitting device. See column 10, line 67 to column 11, line 4, disclosing, "The writing of the brightness information into the pixel PXL is performed by applying an electric signal (data potential Vdata) corresponding to the brightness information to the data line Y in a state wherein the scanning line X is selected." It is understood that a selected scanning line and a data line with brightness information are at a logic level "1".

In regard to claim 3, Sekiya discloses that the control signal uses the scan signal from the next pixel. See column 15, lines 15-18, disclosing an embodiment in which "no special stopping control line is provided, but duty control of the pixels PXL is performed making use of the scanning lines Xl to XN. To this end,.inplace of the stopping control line drive circuit 23, a control circuit 23' is provided separately from the scanning line drive circuit 21." Further see figure 8 and note that control circuit 23' uses scanning lines from the scanning line drive circuit 21. Shigeta also discloses that the light emitting

device unit provides a driving current to the light-emitting device of the next pixel, the discharging unit discharging the light-emitting device (see, 3,lines 30-58).

In regard to claim 4, Sekiya further discloses that the discharging unit discharges the light-emitting device when the scan signal on the next pixel is at a logic level "1" or a high voltage level. See rejection of claim 3 and column 16, lines 17-24, disclosing, "scanning line X is selected when the corresponding output of the control circuit 23' is H (high level) and the vertical clock signal VCK is VCK=H (high level)...the pixels connected to a scanning line X selected by the control circuit 23'stop the emission of light".

In regard to claim 5, Sekiya discloses that the discharging unit is coupled to a ground potential so that electric charges are discharged from the light-emitting device to the ground. Note in figure 1 that the source of TFT3 is connected to ground.

In regard to claim 7, see rejection of claim 1.

In regard to claim 8, Sekiya discloses that the gate terminal of the transistor is connected to the control signal terminal. See rejection of claim 1 and column 11, lines 25-27, disclosing, "The control signal is applied over a stopping control line Z...to the third thing film transistors TFT3". Note in figure 1 that the gate of TFT3 is connected to line Z.

Sekiya further discloses that the drain terminal of the transistor is connected to a ground potential so that electric charges in the light-emitting device discharge to the ground when the transistor is turned on by the control signal. See rejection of claim 5.

Note that the drain of TFT3 is connected to ground when TFT3 receives a control signal at its gate.

In regard to claim 10, see rejection of claim 1.

In regard to claim 12, see rejection of claim 1.

In regard to claim 13, see rejection of claim 2.

In regard to claim 14, see rejection of claim 3.

In regard to claim 15, see rejection of claim 4.

In regard to claim 16, see rejection of claim 5.

In regard to claim 18, see rejection of claim 1.

In regard to claim 19, see rejection of claim 2.

In regard to claim 20, see rejection of claim 3.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiya et al. (6,583,775 B1) in view of Shigeta(6,091,385) and Hack et al. (2002/0030647A1).

In regard to claim 11, Sekiya (as modified by Shigeta) discloses an invention similar to that which is claimed in claim 11. See rejection of claim 1 for similarities. Sekiya does not disclose that the light-emitting device includes a molecular light-emitting diode.

Hack discloses in paragraph [0056], "in the preferred embodiments of the present invention, the phosphorescent emission is produced by the radiative emission from triplet excited states of phosphorescent molecules in the emissive layer. The phosphorescent molecules are excited to their triplet excited states by the energy provided by the recombination of the holes and electrons that are produced in the emissive layer when a voltage is applied across an OLED." These phosphorescent OLEDs are molecular light-emitting diodes, as best understood.

Hack further teaches the use of such phosphorescent OLEDs in paragraph [0013], "There is, in addition, a need to combine these improved lower cost pixel circuits with OLEDs that also have improved performance characteristics. In particular, due to the many benefits and advantages that are provided by OLEDs, especially including overall energy efficiency, there has been much effort in recent years to find materials having still further improved OLED electroluminescent efficiencies... More recent work has demonstrated that OLEDs with higher power efficiencies can be made using organic molecules that emit light from their triplet state, defined as phosphorescence.., phosphorescent OLEDs have a theoretical internal

quantum efficiency of 100% ...As a consequence, since the discovery that phosphorescent materials could be used in an OLED, there has been much interest in developing displays that can effectively utilize the unusually high electroluminescent efficiencies that are possible for phosphorescent OLEDs."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Sekiya by having the light-emitting device include a molecular light-emitting diode, as in the invention of Hack. One would have been motivated to make such a change based on the teaching of Hack that such diodes have "unusually high electroluminescent efficiencies" and "improved performance characteristics".

4. Claims 6, 9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiya et al. (6,583,775 B1) in view of Shigeta (6,091,385) and Filliman (5,255,220).

In regard to claim 6, Sekiya (as modified by Shigeta) discloses an invention similar to that which is disclosed in claim 6. See rejection of claims 1 and 5 for similarities. Note in the rejection of claim 5 that Sekiya discloses that the discharging unit is coupled to a ground potential so that electric charges are discharged from the light-emitting device to the ground. Sekiya does not, however, disclose that the discharging unit is coupled to a negative voltage so that electric charges are discharged from the light-emitting device to the negative voltage terminal.

Filliman discloses an invention in which discharge occurs when a transistor is connected to a negative voltage. See figure 3 and column 6, lines 21-23, disclosing that the transistor Q1 "will discharge the storage node 305 if the write data input row to which terminal 302 is low (i.e., ground or negative)."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Sekiya by having the discharging unit coupled to a negative voltage instead of ground so that the electric charges are discharged from the light-emitting device to the negative voltage terminal, as in the invention of Filliman. One would have been motivated to make such a change based on the teaching of Filliman that discharge will occur to a low terminal, which is also true of the invention of Sekiya, and based on the further teaching of Filliman that such a low terminal is a "ground or negative".

In regard to claims 9 and 17, see rejection of claim 6.

Response to Arguments

5. **Applicant's arguments with respect to claims 1-20 and 24-25 have been considered but are moot in view of the new ground(s) of rejection.**

6. **The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee and Katayama et al are mode of record to show various types of charging and discharging of a lighting element.**

7. **Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Fatahiyar whose telephone number is (571)272-7688. The examiner can normally be reached on Monday-Friday from 9:30 to 6:00.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M. Fatahiyar MF

April 15, 2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600